



MIPS RISC Architecture (2nd Edition)

Gerry Kane, Joseph Heinrich

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A complete reference manual to the MIPS RISC architecture, this book describes the user Instruction Set Architecture (ISA), by the R2000, R3000, R4000, and R6000 (collectively known as the R-Series) processors, together with an extension to this ISA. Focusing on the new R4000 and R6000 chips, this book is organized into two major sections: Chapters 1 through 6 describe the characteristics of the CPU, while Chapter 7 through 9 describe the Floating Point Unit (FPU). This book describes the general characteristics and capabilities of each RISC processor, along with a description of the programming model, memory management unit (MMU), and the registers associated with each processor. Also included is an overview of the underlying concepts that distinguish RISC architecture from Complex Instruction Set Computer (CISC) architecture.

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